APPLICATION

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TITLE: **MITIGATING INTERFERENCE AMONG MULTIPLE RADIO DEVICE TYPES**

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MITIGATING INTERFERENCE AMONG MULTIPLE RADIO DEVICE TYPES

Background

The present invention relates generally to mitigating cross-interference between communication devices in wireless communication systems, and more particularly to systems capable of wirelessly interfacing with several communication device types.

Wireless connectivity for a communication device may be enabled using a medium access control (MAC) and physical layer (PHY) specification within a particular area. Specifically, based on the MAC and PHY specification, access to one or more frequency bands over a communication channel for the purposes of local area communication may be provided. For example, wireless connectivity may be provided to automatic machinery, electronic equipment, or communication devices, which may be fixed, portable, hand-held and/or mobile within a local area.

Although the current focus is on the individual integration of wireless communications technologies into a wireless-enabled platform, it may be beneficial for more than one of these technologies to co-exist in one system. In this way, two or more communication device types may wirelessly interface with a wireless communication system, for example, a wireless-enabled personal computer (PC) system.

A number of short-range and long-range wireless communications technologies, such as Bluetooth or IEEE 802.11, may lend themselves to potential integration with one another in a single wireless communication system. The Bluetooth standard is described in detail in documents entitled "Specifications of the Bluetooth System: Core" and "Specifications of the Bluetooth System: Profiles", both published on July 1999, and are available from the Bluetooth Special Interest Group on the Internet at Bluetooth's official website. The IEEE 802.11 standard is described in detail in a specification entitled "IEEE

Std 802.11 1999 Edition," available from IEEE Customer Service Center, 445 Hoes Lane, P.O. Box 1331, Piscataway, New Jersey 08855-1331.

While these wireless communications technologies have been fairly well defined in the context of individual usage models, their joint usage models with respect to each other are not yet clearly defined. For instance, it is conceivable to have applications where two or more of these communications technologies may have to operate in tandem or concurrently on the wireless-enabled platform.

Unfortunately, such integration may result in undesired interference between the active radio systems, leading to potential signal loss and/or malfunction of the radio system themselves. A cross-interference problem may occur with the integration of multiple radio devices into a wireless communication system, as an example.

Because of the cross-interference problem, integration of wireless communications technologies (e.g., radio frequency (RF) based) into a PC platform may be difficult to accommodate. Therefore, in some cases a simple implementation of multiple integrated radio systems may not be feasible at all. Moreover, based on a certain combination of usage models or other limitations imposed by original equipment manufactures (OEMs), integration of two or more radio technologies into the PC platform may become even more difficult.

A variety of mechanisms have been contemplated to reduce cross-interference problem between multiple radio devices within a system. Traditional ways of dealing with this problem involve circuits for gain control and filter tuning to reject interference signals.

In particular, a set of complex analog circuits is required to obviate the cross-interference. Typically, such complex analog circuits are used for out-of-band frequency rejection using filter tuning, and gain control, using up valuable hardware real estate. Further, a complex signaling mechanism (e.g., sideband signaling) may need to be

deployed in order to support and/or coordinate the filters/gain control circuits, resulting in inefficient usage of available communication bandwidth.

Thus, reduction in cross-interference is desired for communication systems that wirelessly interface with multiple communication devices.

Brief Description of the Drawings

Figure 1 is a block diagram of a wireless communication system including a radio device cross-interference mitigation module, in accordance with one embodiment of the present invention;

Figure 2 is a schematic depiction of a hardware-based wireless communication interface that may be employed in the processor-based wireless communication system of Figure 1 according to one embodiment of the present invention;

Figure 3 is a schematic depiction of a software-based wireless communication interface that may be employed in the processor-based wireless communication system of Figure 1 consistent with one embodiment of the present invention;

Figure 4 is a flow chart of interaction between a controller/scheduler logic and a radio device interface logic in accordance with one embodiment of the present invention; and

Figure 5 is a block diagram of a personal computer platform where the radio device cross-interference mitigation module of Figure 1 may be deployed in accordance with one embodiment of the present invention.

Detailed Description

A wireless communication system 20 includes a module 25 for mitigating cross-interference among disparate wireless devices that may be simultaneously active, in accordance with one embodiment of the present invention. For interfacing, the module 25 may be coupled to a chipset 30 through a shared interface 35. Alternatively, the

module 25 may be advantageously integrated within the chipset 30 itself. In any event, the chipset 30 may comprise a set of integrated circuits, such as a chip 40A and a chip 40B, providing a predetermined functionality based on a particular application, in one embodiment.

In some embodiments, the wireless communication system 20 may be a processor-based system capable of wirelessly interfacing with several radio device types operating in tandem or concurrently on a wireless-enabled platform, such as in personal computing environments. Several short-range and/or long-range wireless communication standards may be deployed. Using the module 25, for example, cross-interference between different types of radio devices 44, a radio device 44A (e.g., operating in accordance with the Bluetooth standard), a radio device 44B (e.g., operating in accordance with the IEEE 802.11 standard), and/or a radio device 44C (e.g., operating in accordance with one or more other wireless standards) may be substantially mitigated.

In one case, the wireless communication system 20 may be a node in a wireless local area network (LAN). Such node may be advantageously positioned proximate to the radio device 44A, for example, a Bluetooth piconet. The Bluetooth piconet may operate in accordance with the Bluetooth specification. Likewise, the radio device 44B may operate in accordance with one of the wireless LAN standards such as the IEEE 802.11 standard.

However, the radio device 44A and the radio device 44B may operate in the same frequency band such as the 2.4 GHz Industrial, Scientific, and Medical (ISM) band which is minimally regulated. The node may employ the module 25 that is responsible for mitigating potential cross-interference between the Bluetooth piconet (which is not part of the wireless LAN that includes the node) and the IEEE 802.11 standard based radio device.

While embodiments according to the Bluetooth and IEEE 802.11 standards are described, the present invention is not limited to such examples. Of course, while using one or more such standards, cross-interference between wireless transceivers in a variety of circumstances and applications may be significantly reduced.

According to one embodiment of the present invention, the module 25 comprises a controller/scheduler 50 to controllably operate a radio device interface 55 including an antenna 60 for carrying out wireless communications. When prompted, the radio device interface 55 may selectively communicate with the radio device 44A, the radio 44B, and/or the radio device 44C. The radio device interface 55 may further comprise a transceiver 65A and transceiver 65B, both operably coupled to the antenna 60 and the controller/scheduler 50. Each transceiver 65 may correspond to a radio device type in one embodiment and provide an activity signal to the controller/scheduler 50.

Essentially, all of the transceivers 65, i.e., within the radio device interface 55, may be disabled while a selected one of the transceivers 65 is conducting communication with a radio device 44, that is, the radio device 44C, as an example. Activity signals from the respective transceivers 65 may be detected at the controller/scheduler 50, indicating some activity corresponding to the radio device 44A and the radio device 44B, respectively.

In particular, when a first communication activity is detected corresponding to the radio device 44A, the transceiver 65A may provide a gating signal 71A to the controller/scheduler 50. Likewise, when a second communication activity is detected corresponding to the radio device 44B, the transceiver 65B may provide a gating signal 71B to the controller/scheduler 50.

Dynamically, a priority may be assigned to each of the transceiver 65 while a potential communication (pending or anticipated) associated with each of the transceiver 65 may be tracked in one embodiment. Control of communication between the transceivers 65, i.e., transceiver 65A through transceiver 65B may then be arbitrated based

on the priority and the potential communications. To this end, one transceiver 65 at a time may then be selectively energized (e.g., powered up or down) based on the control of communication.

For the purposes of handling wireless communications (e.g., radio frequency (RF) communications) and digitally processing such communications, each transceiver may comprise appropriate communication circuitry. That is, as shown in the illustrated embodiment, the transceiver 65A includes an associated RF interface 76A and a baseband interface 78A to enable a first wireless communication 85A between the radio device 44A and the module 25. Similarly to enable a second wireless communication 85B with the radio device 44B, the transceiver 65B may include an associated RF interface 76B and a baseband interface 78B.

Consistent with one embodiment, the radio device interface 55 may further include a channel lock arbitrator 90 being operably coupled to the controller/scheduler 50. For arbitrating control between the first and second wireless communications 85A, 85B, respectively, over a communication channel, a set of shared registers 92, and a set of wireless device specific registers 94 may be provided for the channel lock arbitrator 90.

While the controller/scheduler 50 may be any suitable processor-based unit, in some embodiments, the controller/scheduler 50 may comprise a processor 95, and a storage 97 storing a priority protocol 99. The priority protocol 99, in one embodiment, may include predefined criteria as the basis for assigning a priority to each active transceiver 65. Such predefined criteria may further include a first criterion, a second criterion, and a third criterion.

In one embodiment, the first criterion may be indicative of an overhead associated with a potential communication from/to each transceiver 65. For example, if only a short message is desired to be communicated in compliance with the first criterion of the priority protocol 99, the transceiver 65A may be selected over the transceiver 65B that

having a relatively higher cost of data communications in accordance with one embodiment.

Likewise, the second criterion may indicate to the channel lock arbitrator 90 an amount of data needing transfer which is being associated with the potential communication for each transceiver 65. In some embodiments, communicating a particular amount of data may correspond to an available bandwidth for the transceiver 65, as the transceiver 65A may be relatively slower than the transceiver 65B. Using the priority protocol 99, switching between the transceivers 65 (i.e., the transceivers 65A and 65B) may be advantageously carried out based on the available bandwidth. As an example, in some case, a task of downloading may involve transferring a large chunk of data where an appropriate prioritization may be implemented accordingly.

Alternatively, a priority may be assigned to each transceiver 65 based on the third criterion, indicating a power consumption associated with the potential communication for each transceiver 65. For example, the wireless communication system 20 may be a battery operated system. Moreover, the transceiver 65A may be relatively more power hungry than the transceiver 65B. However, based on an intelligent assessment of the battery's life, the channel lock arbitrator 90 may prioritize the transceiver 65A over the transceiver 65B. Of course, by appropriately employing the priority protocol 99, a suitable prioritization scheme may be devised to usefully fit a specific scenario in a wireless-enabled platform or any other similar application.

In operation, the type of each of the wireless transceivers 65 may be first determined. According to the priority protocol 99, and the type of each wireless transceiver 65, device characteristics and priority information may then be derived. Subsequently, the device characteristics and priority information may be sent to each wireless transceiver 65. Using the set of shared registers 92 and the set of wireless device specific registers 94 of the channel lock arbitrator 90, the control of communication may

be arbitrated by the controller/scheduler 50. That is, in one embodiment, a communication session associated with one of the active wireless transceivers 65 may be selectively enabled. By relinquishing the control of the communication when the communication session is finished, and transferring the control to another one of the active wireless transceiver interfaces when the communication channel becomes available for another communication session, arbitration of the control of the communication may be accomplished, for example, by time slicing (e.g., allocating available time slots of the communication channel to Bluetooth and IEEE 802.11 transmissions where, for example, the Bluetooth time slots may further be shared among more than one active Bluetooth piconets). As a result, cross-interference between, the transceiver 65A and the transceiver 65B may be substantially mitigated.

Although not shown, in accordance with one embodiment, each transceiver 65 may further include a physical layer unit (PHYU), such as a modulator/demodulator (MODEM) and a medium access control unit (MACU) compliant with a desired standard (e.g., Bluetooth or IEEE 802.11). The physical layer unit may receive a received signal strength indication (RSSI) signal from the physical layer unit. The RSSI signal is conventionally utilized in association with what is known as a channel access control. The module 25 uses the raw RSSI data, received from the physical layer unit. The module 25 uses the RSSI data to detect transmission of any radio or wireless devices that are not part of the wireless LAN, such as transmission from a Bluetooth piconet.

A hardware-based wireless communication interface 110 is shown in Figure 2 that may be employed in the wireless communication system 20 of Figure 1 according to one embodiment of the present invention. In this case, a communication device 115A and a communication device 115B may interface with a PC chipset 120A through a shared bus 125. A controller 50A coupled to both the communication device 115A and the communication device 115B may control at least in part any radio communication

activity at each communication device. To this end, each communication device may provide a signal to the controller 50A indicating local communication activity.

More specifically, the communication device 115A sends a control signal 135A to the controller 50A. Likewise, the communication device 115B sends a control signal 135B to the controller 50A. Both the control signals 135, that is, the control signal 135A and the control signal 135B in the illustrated embodiment may provide to the controller 50A an indication of a communication activity that is either pending, anticipated or undergoing. In one case, based on a control message sent by the PC chipset 120A via the shared bus 125 to the communication device 115A and/or the communication device 115B, individual radio communication activity may be selectively controlled by the controller 50A.

The communication device 115A, in one embodiment, comprises a baseband interface unit 140A and a radio communication interface 142A. In the same manner, the communication device 115B also includes a baseband interface unit 140B and a radio communication interface 142B.

When the controller 50A detects that both of the communication devices 115, (that is, the communication device 115A and the communication device 115B in the depicted embodiment) are active and seeking a communication channel, the control of the communication channel may be arbitrated between the two. In one embodiment, the controller 50A powers down the non-active communication device 115 that was denied the control of the communication channel. In this way, since only one of the two communication devices 115 may be operational at a particular time, cross-interference between the two communication devices 115 may be substantially mitigated.

A software-based wireless communication interface 150 shown in Figure 3 may be employed in the wireless communication system 20 of Figure 1 in one embodiment consistent with the present invention. The software-based wireless communication

interface 150 may include a scheduler 50B and a shared memory 160 according to one embodiment. Using the shared memory 160, the scheduler 50B may arbitrate the control of a communication channel between the radio subsystem 162A and the radio subsystem 162B. According to one embodiment, while the radio subsystem 162A may comprise a transceiver 165A, the radio subsystem 162B may include a transceiver 165B to enable bi-directional communications.

When a communication activity occurs in the transceiver 165A, the radio subsystem 162A may provide a gating signal 170A to the scheduler 50B according to one operation of the present invention. Similarly, the radio subsystem 162B may provide a gating signal 170B to the scheduler 50B when another communication activity occurs at the transceiver 165B. In any case, however, both the radio subsystems 162 may employ the shared memory 160 to inform each other about the respective communication activities, which may be either pending, anticipated, or undergoing.

In one embodiment, the shared memory 160 includes a set of global registers 175 and a set of dedicated registers 177A through 177B for facilitating arbitration of the control of the communication channel between the two radio subsystems 162A and 162B. For example, the radio subsystems 162A and 162B may use a shared memory architecture in a semaphore-based implementation according to one embodiment. Such implementation may enable selective blocking off the transmission/reception of a radio communication at the transceiver 165A and/or the transceiver 165B.

In this manner, a selective communication control may be provided to the radio subsystem 162A and the radio subsystem 162B by the scheduler 50B. While the radio subsystem 162A is active, the radio subsystem 162B may be powered down in order for the radio subsystem 162A to continue communication, avoiding cross-interference, as an example.

A PC chipset 120B may also use the shared memory 160 to control at least a portion of the communications from the radio subsystem 162A and the radio subsystem 162B. The scheduler 50B, using the shared memory 160, may provide a global lock feature based on the contents of the global resistors 175 and the registers REG 177A through REG 177B. For example, if both the radio subsystems 162A and 162B attempt to acquire the control of the communication channel, a first indication may be provided in the global registers 175 and a second indication into a local register of the registers REG 177A through REG 177B dedicated to that particular radio subsystem.

Specifically, when the radio subsystem 162A may be given the control of the communication channel a bit may be set in REG 177A. In this way, access to the communication channel may be selectively provided to the radio subsystems 162A and 162B. If a conflict concerning a communication channel control arises, the scheduler 50B may inform the non-active radio subsystem regarding the activity of the active radio subsystem through the global registers 175. For example, if the radio subsystem 162A is active and the radio subsystem 162B desires the control of the communication channel, the scheduler 50B arbitrates such control of the communication channel by indicating to the radio subsystem 162B about the current ownership of the communication channel by the radio subsystem 162.

All of the radio subsystems 162A through 162B may remain in a low power state or in a power down mode until given the ownership of the communication channel. When the radio subsystem 162A is finished communicating and using the global registers 175, an indication may be provided in the shared memory 160 for the radio subsystem 162B to inform that the communication channel is now available.

In one embodiment, one or more access bits may be set in the global registers 175 and registers REG 177A through REG 177B, for the purposes of generating an indication for/by the scheduler 50B as well as the radio subsystem 162A and the radio subsystem

162B. These access bits may inform the scheduler 50B as well as the radio subsystems 162 regarding a non-active state and seeking of the control of the communication channel.

To mitigate cross-interference among radio devices, a controller/scheduler logic 50C (for example, the controller/scheduler 50 of Figure 1) and a radio device interface logic 55A (for example, the radio device interface 55 of Figure 1) consistent with one embodiment of the present invention is shown in Figure 4. A hypothetical dotted line 210 functionally distinguishes the controller/scheduler logic 50C from the radio device interface logic 55A, according to one embodiment. Of course, based on a particular application a desired configuration of the controller/scheduler logic 50C and the radio device interface logic 55A may be suitably deployed.

Interaction between the controller/scheduler logic 50C and the radio device interface logic 55A enables arbitration of a communication channel in accordance with one embodiment of the present invention. Each radio device interface may provide a gating signal to the controller/scheduler logic 50C at block 210. A gating signal may be detected from the radio device interface associated with an active wireless device at 215. Based on the determination of an acceptable radio device interface type at diamond 220, the controller/scheduler logic 50C may proceed to further identify a specific type of the radio device interface.

When the radio device interface type is determined to be a type A radio device interface at diamond 225, the controller/scheduler logic 50C may proceed to the next step. Otherwise, if at diamond 230, a type B radio device interface is determined, then again, the controller/scheduler logic 50C proceeds to the next step. Likewise, if the radio device interface is determined to be of a type C, the controller/scheduler logic 50C proceeds to the next step as well.

In the event that the radio device interface type is found to be unidentifiable, the controller/scheduler logic 50C may terminate. After at least two active radio device interface types are recognized, a priority may be assigned to each such active radio device interface type at block 240. Device characteristics and priority information may then be prepared and subsequently sent to each active radio device interface type at block 245. By querying the controller/scheduler logic 50C, the radio device interface logic 55A may request a channel lock at block 250 for communicating with an associated active wireless device.

Based on the device characteristics and the priority information, in response to one or more channel lock queries, the controller/scheduler logic 50C may provide the channel lock to a selected one of the active device interface at block 255. Thus, the selected active radio device interface type at block 260 may gain ownership of the channel lock. All the active radio device interface types associated with the active wireless devices except the one provided the channel lock may be de-energized (e.g., powered down) at block 265. Once the ownership of the channel lock is gained by the radio device interface logic 55A, a communication channel may be opened at block 270. Therefore, the active wireless device corresponding to the selected active radio device interface type may communicate at block 275.

Once the communication is completed, a determination is made as to whether the selected active wireless device may need to further use the communication channel at diamond 280. If not, the ownership of the channel lock may be released at block 285. In the case another transaction, i.e., more communication (e.g., transmission/reception) is desired, the control may again be provided by the controller/scheduler logic 50C. At this time, new device characteristic and new priority information, which may be dynamically generated in real time, sent to each active ratio device interface type. Conversely, if no

potential communication is queued, the controller/scheduler logic 50C completes its current iteration.

A personal computer (PC) platform/system 300 as shown in Figure 5 includes a PC chipset 120C and a processor 310. With the PC chipset 120C, the processor 95A interfaces through a shared bus 315. The shared bus 315 may further be coupled to the bridge chip 320. A memory 325 and a system read only memory (ROM) in conjunction with a basic input output system (BIOS) 330 may further be coupled to the bridge chip 320. Using a secondary bus 335, the bridge chip 320 may interface with a radio device cross-interference mitigation module 25A.

Generally, this module 25A may be deployed in the PC platform/system 300 in accordance with any desired wireless communication standard. However, the actual mechanism implemented for cross-interference reduction likely depend on the implementation guidelines (e.g., based on a specific wireless communication standard) for a given communications architecture for a particular PC system.

Several factors may be considered while designing a multi-radio control algorithm for interference mitigation based on a particular embodiment of the present invention. For example, order of priority for transmission/reception for the radio systems available may be pre-programmed. Moreover, criteria on the relative states of the different radio system with respect to each other may be incorporated in advance. Additionally, potential limitations dictated by the platform operating modes (or power management) may also be taken in consideration in some cases.

Therefore, in a PC system having integrated RF and baseband hardware may anticipate activity on any available radio device and use this information to intelligently control the other radio devices to reduce interference. Advantageously, complex radio filter circuits may be avoided along with sideband signaling circuitry to support the

filters/gain control circuits may be rendered unnecessary when cross-interference may be controlled according to one embodiment of the present invention.

While the present invention has been described with respect to a limited number of embodiments, those skilled in the art will appreciate numerous modifications and variations therefrom. It is intended that the appended claims cover all such modifications and variations as fall within the true spirit and scope of this present invention.

What is claimed is: